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(54) Title of the Invention: DISPLAY DEVICE OF

5 FLUORESCENT DISPLAY TUBE

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Specification

15 1. Title of the Invention:

DISPLAY DEVICE OF FLUORESCENT DISPLAY TUBE

2. Claim:

A display device of a fluorescent display tube,
20 comprising a microcomputer in a control unit, a supply
monitor circuit for detecting a supply voltage of the
microcomputer and controlling an output at a given
voltage value, a reset circuit connected to the supply
monitor circuit for outputting a reset pulse having a
25 predetermined width at an output of the supply monitor
circuit, a shift register for shifting a signal from
the microcomputer, a scanning signal monitor circuit

connected to the shift register for monitoring scanning signals at predetermined intervals, a drive circuit connected to an output of the shift register for driving the fluorescent display tube, and a blank 5 circuit for obtaining a logical sum of an output of the supply monitor circuit, an output of the reset circuit, an output of the scanning signal monitor circuit, and a blank signal output from the microcomputer, and turning off an output of the drive circuit.

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3. Detailed Description of the Invention:

(1) Description of the Field of the Invention

The present invention relates to a blank circuit of a display device of a fluorescent display tube.

15 (2) Description of the Prior Art

In a display device using a microcomputer in a control circuit, several tens of milliseconds are required to reset the microcomputer, and during the resetting process, the microcomputer is placed in an 20 operation stopped state. Additionally, the microcomputer can have a program running away by the fluctuation of a supply voltage, etc. Therefore, a reset circuit for outputting a reset pulse having a width of several tens of milliseconds when power is 25 turned on and when power fluctuates using a supply voltage monitor circuit is used. Meanwhile, since a fluorescent display tube is designed for time division

drive, a data signal and a scanning signal are output to a shift register from the microcomputer, and is applied to the fluorescent display tube through a drive circuit, thereby obtain desired display. When display 5 is shifted from a digit to the next digit during time division drive, signals can overlap and cause some flicker. Therefore, before or after the digit shift, the microcomputer outputs a blanking pulse for temporarily stopping the drive circuit to avoid flicker.

10 In the time division drive, when the time division stops for any reason, a voltage can be concentrated on a specific digit and degrade a fluorescent display tube. Therefore, means for stopping the drive when scanning is stopped is adopted using a monitor circuit of a 15 scanning signal.

With the above-mentioned configuration of the display device, there has been the disadvantage of a failure of wrong display on a fluorescent display tube, abnormal emission, etc. when power is turned on or off, 20 when a supply voltage is abnormally low, or when a microcomputer is reset.

(3) Object of the Invention

The present invention aims at overcoming the 25 above-mentioned disadvantage, and providing a display device of a fluorescent display tube having a blank circuit for obtaining a logical sum of blank signal

output from the above-mentioned supply monitor circuit, reset circuit, scanning signal monitor circuit, and microcomputer, and turning off the output of the drive circuit.

5 (4) Description of Configuration and Operation of the Invention

Figure 1 is a block diagram of a fluorescent display tube showing an embodiment of the present invention. The fluorescent display tube includes a
10 microcomputer 1, a supply monitor circuit 2, a reset circuit 3, a shift register 4 for data signal, a scanning signal shift register 5, a scanning signal monitor circuit 6, a blank circuit 7 of the present invention, a drive circuit 8 of a data signal, a
15 control circuit 9 for a scanning signal, and a fluorescent display tube 10.

Described below is the operation of the fluorescent display tube. Based on a value for monitor of a voltage value of power, that is, normally a
20 voltage value at which the microcomputer 1 can start an operation, the supply monitor circuit 2 outputs a positive signal when a voltage is lower than the value, and outputs a negative signal when the voltage is equal to or larger than the value. The signal output 21 is
25 applied to the reset circuit 3. The reset circuit 3 is configured by a monostable multivibrator, and outputs a reset pulse 31 of several tens of milliseconds at the

output signal 21 of the supply monitor circuit 2. The microcomputer 1 receives the reset pulse 31, and outputs a display data signal 11, a scanning signal 12 for time division drive, and a blanking pulse 13. The 5 display data signal 11 is connected to the shift register 4 and serial-to-parallel converted, and a parallel output 41 is applied to the drive circuit 8 and is converted to a driving voltage by the drive circuit 8, and the output 81 is applied to the data 10 electrode of the fluorescent display tube 10. On the other hand, the scanning signal 12 is connected to the shift register 5, the shift register 5 serial-to-parallel converts the signal, the parallel output 52 is applied to the control circuit 9 and converted to a 15 driving voltage, and the output 91 is applied to the scanning electrode of the fluorescent display tube 10. The serial output 51 of the shift register 5 is applied to the scanning signal monitor circuit 6. The scanning signal monitor circuit 6 is a monostable multicircuit, 20 and outputs the first scanning signal, that is, a negative signal 61. The negative pulse signal 61 is retriggered by the second and subsequent scanning signals, held as negative while a scanning signal is normally output, and turned to positive when the 25 scanning signal stops. The blank circuit 7 receives the signal output 61 from the scanning signal monitor circuit 6, the blanking signal 13 from the

microcomputer 1, an output 22 from the supply monitor circuit 2, and an output 32 from the reset circuit 3, obtains a logical sum, and outputs the signal 71. The drive circuits 8 and 9 are three-state drive circuit, 5 and its output is controlled by the logical sum output signal 71.

Figure 2 is a view showing the logic of the first embodiment of the blank circuit 7. The input 13 is a blanking signal from the microcomputer 1, and turns to 10 a high level when the display is to be blank, and to a low level when it is to be displayed. The input 22 is a signal from the supply monitor circuit 2, and turns to the low level when power is in a normal state, and to the high level when it is in an abnormal state. The 15 input 32 is a signal from the reset circuit 3, and turns to the high level in the resetting period, and otherwise in the low level. The input 61 is a signal from the scanning signal monitor circuit 6, and enters the low level in the normal state, and the high level 20 in the abnormal state. The output 71 is a high level signal if any of the inputs 13, 22, 32, and 61 is a high level. As described above, since the output of the drive circuits 8 and 9 can be controlled by a control input terminal, the display can be set to be 25 blank if any of the inputs 13, 22, 32, and 61 is in the high level by connecting the logical sum output 71.

(5) Description of the Effect

As described above, the display can be blank when a supply voltage is abnormal, during the reset period of the microcomputer, or when a scanning signal is in an abnormal state. Therefore, a display device of a 5 fluorescent display tube can suppress the failure such as wrong display, abnormal emission, etc. on the fluorescent display tube even when power is turned on and off and the supply voltage is abnormally low.

10 4. Brief Description of the Drawings:

Figure 1 is a block diagram of the display device of the fluorescent display tube showing an embodiment of the present invention. Figure 2 shows the logic indicating an embodiment of the blank circuit of the 15 present invention.

1 ... Microcomputer, 2 ... Supply monitor circuit, 3 ... Reset circuit, 4, 5 ... Shift register, 6 ... Scanning signal monitor circuit, 7 ... Blank circuit, 8, 9 ... Drive circuit, 10 ... Fluorescent display tube, 11 ...
20 Data signal output, 12 ... Scanning signal output, 13 ... Blank signal output, 21, 22 ... Supply monitor circuit signal output, 31, 32 ... Reset pulse output, 41 ... Parallel output of shift register 4, 51 ... Serial output of shift register 5, 52 ... Parallel
25 output of shift register 5, 61... Scanning signal monitor signal output, 71 ... Logical sum signal output, 81 ... Drive output of the drive circuit 8, 91 ...

Drive output of the control circuit 9.

なら、ハイレベル信号が出力される。前述したように駆動回路8, 9は制御入力端子で出力がコントロール出来るので、論理和出力71を接続することにより入力13, 22, 32, 61のいずれか1つでもハイレベルなら、表示をブランクすることが出来る。

(5) 効果の説明

以上説明したように、電源電圧が異常のときや、マイクロコンピュータのリセット期間中や、走査信号異常時に表示をブランクできるので、電源のオン・オフ時や電源電圧の異常低下時においても蛍光表示管が、データを表示や異常発光する等の不具合を防ぐことが出来る蛍光表示管の表示装置が得られる。

4. 図面の簡単な説明

第1図は本発明の一実施例を示す蛍光表示管の表示装置のブロック図である。第2図は本発明のブランク回路の一実施例を表わす論理回路図である。

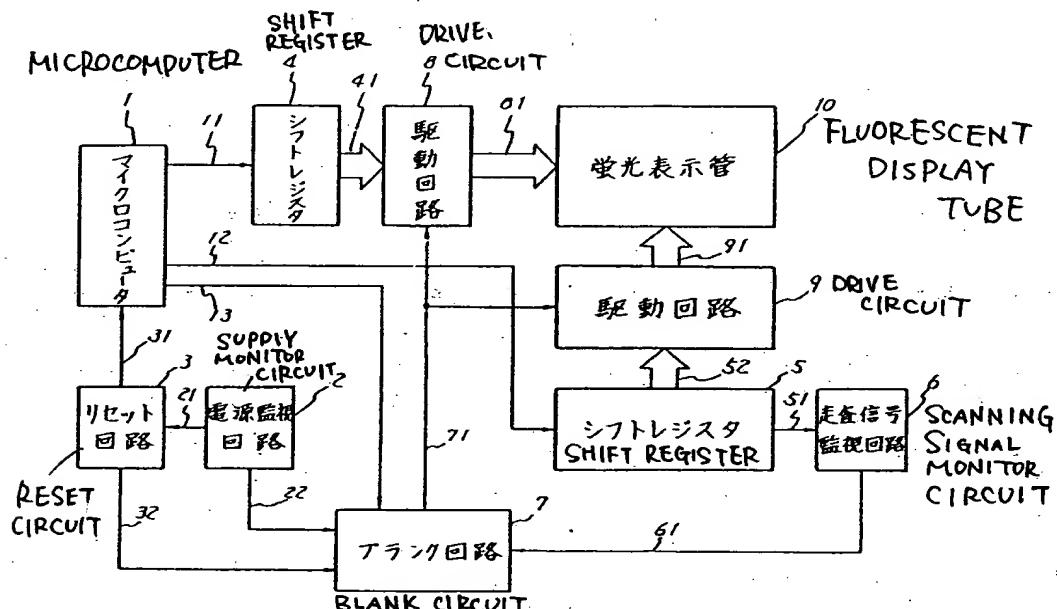
1 ……マイクロコンピュータ、2 ……電源監視回

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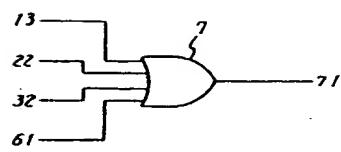
- 8 -

路、3 ……リセット回路、4, 5 ……シフトレジスタ、6 ……走査信号監視回路、7 ……ブランク回路、8, 9 ……駆動回路、10 ……蛍光表示管、11 ……データ信号出力、12 ……走査信号出力、13 ……ブランク信号出力、21, 22 ……電源監視回路信号出力、31, 32 ……リセットパルス出力、41 ……シフトレジスタ4の並列出力、51 ……シフトレジスタ5の直列出力、52 ……シフトレジスタ5の並列出力、61 ……走査信号監視回路信号出力、71 ……論理和信号出力、81 ……駆動回路8の駆動出力、91 ……駆動回路9の駆動出力。

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第1図 [FIG.1]



第2図 FIG. 2